



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,493	12/31/2001	Ming Qiu	7294-70335-01	5525

24197 7590 03/26/2007
KLARQUIST SPARKMAN, LLP
121 SW SALMON STREET
SUITE 1600
PORTLAND, OR 97204

EXAMINER

HUYNH, KIM T

ART UNIT	PAPER NUMBER
----------	--------------

2111

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/038,493

Applicant(s)

QIU, MING

Examiner

Kim T. Huynh

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 December 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15 and 18-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15 and 18-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 15, 18-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wachel (Pub. No. US2040148448) in view of Hill et al. (US Patent 6,578,103)

As per claim 15, Wachel discloses a high-density server (fig.1, 100 ie system 100) comprising:

a midplane board (fig.1, 110) having opposing front and back sides;
(paragraph 34)

multiple processor cards (fig.1, 119 ie main cards) physically and electrically connected to the midplane board; (paragraph 36-37)

multiple network control cards(fig.1, 116 ie switch card) physically and electrically connected to the midplane board; and (paragraph 36-37)

multiple power supply cards (paragraph 37) physically and electrically connected to the midplane board wherein the multiple processor cards, the multiple network control cards and the multiple power supply cards are connected to the midplane board via CompactPCI connectors (paragraph 29-31)

Wachel discloses all the limitations as above except wherein the at least some of the multiple processor cards have pinout definitions the mirror image of J1 CompactPCI front side pinout definitions. However, Hill discloses certain compactPCI boards may be devoid of a connector or mating portion, at a J4 location that would otherwise be coupled to a P4 connector. The backplane is configured in such way that compactPci boards devoid of J4 connectors are still compatible with the backplane and may be used in the system similarly to compactPCI boards that include a compatible connector at the J4 location. (col.3, lines 45-65)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hill's teaching into Wachel's system so as to provide a bus architecture that is compatible with existing PCI and compactPCI hardware that can transfer much larger amounts of data than currently available to allow more users to use a single system. (col.2, lines 5-12)

As per claim 18, Wachel discloses wherein pin connectors are attached to the midplane board and socket connectors are attached to the multiple processor cards, the multiple network control cards and the multiple power supply cards and wherein pins of the pin connectors are secured into sockets of the socket connectors to physically and electrically connect the multiple processor cards, multiple network control cards and multiple power supply cards to the midplane board. (paragraph 29, 31-33)

As per claim 19, Wachel discloses the high-density server further comprising a KMV switch physically and electrically connected to the midplane board.
(paragraph 35)

As per claim 20, Wachel discloses the high-density server further comprising multiple fiber channel hard drive cards physically and electrically connected to the midplane board. (paragraph 37)

As per claim 21, Wachel discloses wherein the multiple network control cards are selected from the group consisting of a network switch, a network hub, a fiber channel arbitrate loop hub and a fiber channel arbitrate loop switch. (paragraph 38, ie switched Ethernet)

As per claim 22, Wachel discloses wherein at least one of the multiple processor cards controls at least two expansion cards through a J1 portion of the Compact PCI connectors. (paragraph 35)

As per claim 23, Wachel discloses the high-density server further comprising conductive traces extending along the midplane board to electrically connect the multiple processor cards, multiple network control cards and multiple power supply cards through J2 portions of the CompactPCI connectors. (paragraph 29)

Art Unit: 2111

As per claim 24, Wachel discloses wherein the multiple network control cards control through the J2 portions of the CompactPCI connectors a network formed from the multiple processor cards, multiple network control cards, the multiple power supply cards and the connecting conductive traces. (paragraph 29, 31-33)

As per claim 25, Wachel discloses wherein the conductive traces connect the multiple processor cards, multiple network control cards, and multiple power supply cards in a daisy-chain or a star network configuration. (paragraph 29, ie network communication links)

As per claim 26, Wachel discloses the server further including a chassis enclosing the midplane board, the multiple processor cards, the multiple network control cards, and the multiple power supply cards. (paragraph 29)

As per claim 27, Wachel discloses wherein the rocessor cards, the network control cards and the power supply cards are hot swappable so that any of the cards can be replaced without shutting down the network. (paragraph 28)

As per claim 28, Wachel discloses wherein the network will continue to operate even if any one of the multiple processor cards, the multiple network control cards and the multiple power supply cards fails to operate. (paragraph 28, 40)

Art Unit: 2111

3. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wachel (Pub. No. US2040148448) in view of Hill et al. (US Patent 6,578,103) and further in view of Loder et al. (Pub. No. US2005/0018973)

The indicated allowability of claims 29-30 is withdrawn in view of the newly discovered reference(s) to Loder et al. (Pub. No. US2005/0018973). Rejections based on the newly cited reference(s) follow.

Wachel discloses a high-density server comprising:

a midplane board (fig.1, 110) having opposing front and back sides;
(paragraph 34)

multiple processor cards(fig.1, 119 ie main cards) physically and electrically connected to the midplane board;(paragraph 36-37)

multiple network control cards (fig.1, 116 ie switch card) physically and electrically connected to the midplane board. (paragraph 36-37)

Wachel discloses all the limitations as above except wherein the at least some of the multiple processor cards have pinout definitions the mirror image of J1 CompactPCI front side pinout definitions. However, Hill discloses certain compactPCI boards may be devoid of a connector or mating portion, at a J4 location that would otherwise be coupled to a P4 connector. The backplane is configured in such way that compactPci boards devoid of J4 connectors are still compatible with the backplane and may be used in the system similarly to compactPCI boards that include a compatible connector at the J4 location. (col.3, lines 45-65)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hill's teaching into Wachel's system so as to provide a bus architecture that is compatible with existing PCI and compactPCI hardware that can transfer much larger amounts of data than currently available to allow more users to use a single system. (col.2, lines 5-12)

Furthermore, the modified of Wachel disclose all the limitations as above except wherein the front and back sides of the midplane board are substantially rectangular with a longer edge of the rectangle defining an x-axis, the multiple processor cards have a processor card front and a processor card backside, wherein the shorter edge of the multiple processor cards defines a y-axis; and wherein at least some of the multiple processor cards are physically connected to the midplane board in a vertical configuration so that the y-axis defined by the shorter edge of the multiple processor cards is substantially perpendicular to the x-axis defined by the longer edge of the midplane board. However, Loder discloses the axis of interconnections is called the longitudinal or x-axis and is defined by the longitudinal alignment of the optical fibers at the point of connection. Generally, in backplane applications, the longitudinal axis is collinear with the axis of movement of the cards and the axis of connection of the fibers in and out of the cabinets. The y-axis is defined by the perpendicular to the x-axis and the planar surface of the card. (paragraph 10) It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Loder's teaching into the modified of Wachel's system so as to

provide an improvement for controlling interconnection of number of optical fiber system. (paragraph 22)

Response to Amendment

4. Applicant's amendment filed on 12/22/06 have been fully considered but does not place the application in condition for allowance.

a. In response to applicant's arguments that Hill does not cure the deficiencies of Wachel, "wherein the at least some of the multiple processor cards have pinout definitions the mirror image of J1 CompactPCI front side pinout definitions". Examiner respectfully disagrees. As Hill notes at (col.3, lines 45-63), certain boards (ie multiple processor cards) may devoid or mating portion(pinout definitions) at J4 location. The backplane is configured in such way that the boards devoid of J4 are compatible (mirror image) with the backplane and compatible connector at the J4 location. It is clear that it reads on the breadth of the claimed languages therefore it is properly stated in the rejection of record.

b. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Examiner relies on Hill's reference the teaching of the multiple processor cards have pinout definitions

the mirror image of J1 CompactPCI front side pinout definitions for combination. As Hill notes at (col.3, lines 45-63), certain boards (ie multiple processor cards) may devoid or mating portion(pinout definitions) at J4 location. The backplane is configured in such way that the boards devoid of J4 are compatible (mirror image) with the backplane and compatible connector at the J4 location. In that (abstract) Hill's purpose is to provide a method of directly transferring data across PCI backplane. Since Wachel's purpose is to improve information transfer data rates among all the cards in a rack. It would been obvious to one of ordinary skill in the art at the time the invention was made so as provide larger amounts of data available to allow more users to use. Thus, it is clear that Hill is analogous art and therefore properly combinable for the purpose stated in the rejection of record.

Conclusion

5. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9:00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at (571)272-3632 or via e-mail addressed to [mark.rinehart@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

March 14, 2007


MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100